This listing of claims will replace all prior versions, and listings, of claims in the application:

II. Listing of Claims:

Claims 1-31 (Cancelled)

Claim 32 (Currently Amended): A structure ~~that includes a MOSFET which is a low power device formed on a first device area and an adjacent MOSFET which is a high performance device formed on a second device area on a substrate~~ having a first device in a first area and a second device in a second area on a substrate, comprising:

~~a substrate having shallow trench isolation (STI) regions that separate a first device area from a second device area, said first and second device areas include lightly doped and heavily doped source /drain regions;~~

an interfacial layer having a first thickness formed on said first ~~device~~ area;

a high dielectric-constant (k) dielectric stack having a second thickness formed on said interfacial layer;

a first gate electrode ~~with a spacer on each of its two sides~~ formed on said high k dielectric stack;

an ultra thin dielectric layer having a third thickness disposed on the second region; and

a second gate electrode ~~with a spacer on each of its two sides~~ formed on said ultra thin dielectric layer.

Claim 33 (currently amended): The structure of claim 32 wherein the interfacial layer is comprised of silicon nitride, silicon oxide, or silicon oxynitride ~~with a thickness between 0 and about 30 angstroms~~.

Claim 34 (Previously presented): The structure of claim 32 wherein the high k dielectric stack is comprised of one or more of Ta_2O_5, TiO_2, Al_2O_3, ZrO_2, HfO_2, Y_2O_3, L_2O_3, and their aluminates and silicates.

Claim 35 (Currently amended): The structure of claim 32 wherein ~~the thickness of the high k dielectric stack~~ the second thickness is from about 15 to 100 angstroms.

Claim 36 (Previously presented): The structure of claim 32 wherein the first and second gate electrodes are comprised of doped or undoped polysilicon.

Claim 37 (Previously presented): The structure of claim 32 wherein the ultra thin dielectric layer is comprised of silicon oxide or silicon oxynitride with an effective oxide thickness of less than 10 angstrom.

Claim 38 (Previously presented): The structure of claim 32 wherein the ultra thin dielectric layer is silicon oxynitride and the high k dielectric stack is comprised of ZrO_2 and Al_2O_3.

Claim 39 (Previously presented): The structure of claim 32 wherein the ultra thin dielectric layer is SiO_2 and the high k dielectric stack is comprised of HfO_2.

Claim 40 (Previously presented): The structure of claim 32 further comprising a silicide layer formed on the gate electrode layer and on the semiconductor substrate about heavily doped source/drain regions.

Claim 41 (Currently amended): A structure ~~that includes a MOSFET which is a low power device formed on a first device area, a MOSFET which is a high performance device formed on a second device area, and a MOSFET which is a I/O device formed on a third device area on a substrate~~ having a first device in a first area, a second device in a second area, and a third device in a third area on a semiconductor substrate, comprising:

~~a substrate having first, second, and third device areas and shallow trench isolation (STI) regions that separate adjacent device areas, said first, second, and third device areas include lightly doped and heavily doped source /drain regions;~~

an interfacial layer having a first thickness formed on said first ~~device~~ area;

a high dielectric-constant (k) dielectric stack having a second thickness formed on said interfacial layer;

a first gate electrode ~~with a spacer on each of its two sides~~ formed on said high k dielectric stack;

an ultra thin dielectric layer having a third thickness formed on the second ~~device~~ area;

a second gate electrode ~~with a spacer on each of its two sides~~ formed on said ultra thin dielectric layer;

a second gate dielectric layer having a fourth thickness formed on said third ~~device~~ area; and

a third gate electrode ~~with a spacer on each of its two sides~~ formed on said second dielectric layer.

Claim 42 (Currently amended): The structure of claim 41 wherein the interfacial layer is comprised of silicon nitride, silicon oxide, or silicon oxynitride with a thickness ~~of between 0 and~~ up to about 30 angstrom.

Claim 43 (Previously presented): The structure of claim 41 wherein the high k dielectric stack is comprised of one or more of Ta_2O_5, TiO_2, Al_2O_3, ZrO_2, HfO_2, Y_2O_3, L_2O_3, and their aluminates and silicates.

Claim 44 (Currently amended): The structure of claim 41 wherein ~~the thickness of the high k dielectric stack~~ the second thickness is from about 15 to 100 angstroms.

Claim 45 (Previously presented): The structure of claim 41 wherein said first, second, and third gate electrodes are comprised of doped or undoped polysilicon.

Claim 46 (Previously presented): The structure of claim 41 wherein the ultra thin dielectric layer is comprised of silicon oxide or silicon oxynitride with an effective oxide thickness of less

than 10 angstrom.

Claim 47 (Previously presented): The structure of claim 41 wherein the second dielectric layer is SiO_2 with a thickness from about 10 to 100 angstrom.

Claim 48 (Previously presented): The structure of claim 41 wherein the ultra thin dielectric layer is silicon oxynitride and the high k dielectric stack is comprised of ZrO_2 and Al_2O_3.

Claim 49 (Previously presented): The structure of claim 41 wherein the ultra thin dielectric layer is SiO_2 and the high k dielectric stack is comprised of HfO_2.

Claim 50 (Currently amended): The structure of claim 41 further ~~comprised of~~ comprising a silicide layer formed on said substrate above heavily doped source/drain regions and on said first, second, and third gate electrodes.

Claim 51 (new): The structure of claim 32 wherein the first device comprises a low power device and the second device comprises a high performance device.

Claim 52 (new): The structure of claim 32 wherein the first thickness is up to about 30 angstrom.

Claim 53 (new): The structure of claim 41 wherein the first device comprises a low power device, the second device comprises a high performance device, and the third device comprises an input/output device.

Claim 54 (Previously Presented as Claim 32): A structure that includes a MOSFET which is a low power device formed on a first device area and an adjacent MOSFET which is a high performance device formed on a second device area on a substrate, comprising:

a substrate having shallow trench isolation (STI) regions that separate a first device area from a second device area, said first and second device areas include lightly doped and heavily doped source /drain regions;

an interfacial layer having a first thickness formed on said first device area;

a high k dielectric stack having a second thickness formed on said interfacial layer;

a first gate electrode with a spacer on each of its two sides formed on said high k dielectric stack;

an ultra thin dielectric layer having a third thickness disposed on the second region; and

a second gate electrode with a spacer on each of its two sides formed on said ultra thin dielectric layer.